

ST17H66B2

Bluetooth Low Energy System on Chip with SIG-Mesh

Key Features

- High-performance low-power 32-bit processor
- Memory
 - 256KB SPI NOR flash memory
 - 64KB SRAM, all programmable retention in sleep mode
 - 4-way instruction cache with 8KB Cache RAM
 - 96KB ROM
 - 256bit efuse
- 11 general purpose I/O pins
 - GPIO status retention in off/sleep mode
 - configurable as serial interface and programmable IO MUX function mapping
 - All pins can be configured for wake-up
 - All pins for triggering interrupt
 - 3 quadrature decoder(QDEC)
 - 6-channel PWM
 - 2-channel PDM/I2C/SPI/UART
 - 4-channel DMA
- DMIC/AMIC with microphone bias
- 5-channel 12bit ADC with low noise voicePGA
- 6-channel 24bit timer, one watchdog timer
- Real timer counter (RTC)
- Power, clock, reset controller
- Flexible power management
 - Operating Voltage range 1.8V to 3.6V
 - Battery monitor
- Power consumption
 - 0.3 μ A @ OFF Mode(IO wake up only)
 - 1 μ A @ Sleep Mode with 32KHz RTC
 - 4 μ A @ Sleep Mode with 32KHz RTC and all SRAM retention
 - Receive mode: 8mA @3.3V power supply
 - Transmit mode: 8.6mA(0dBm output power) @3.3V power supply
 - MCU: <90 μ A/MHz
- RC oscillator hardware calibrations
 - Internal High/Low frequency RC osc
 - 32KHz RC osc for RTC with +/-500ppm accuracy
 - 32MHz RC osc for HCLK with 3% accuracy
- High Speed Throughput
 - Support BLE 2Mbps Protocol
 - Support Data Length Extension
 - Throughput up to 1.6Mbps(DLE+2Mbps)
- BLE 5.2 feature
- AoA/AoD Direction Finding
- Support SIG-Mesh Multi-Feature
 - Friend Node
 - Low Power Node
 - Proxy Node
 - Relay Node
- 2.4 GHz transceiver
 - Compliant to Bluetooth 5.2
 - Sensitivity:
 - 97dBm@BLE 1Mbps data rate
 - 103dBm@BLE 125Kbps data rate
 - TX Power -20 to +10dBm in 3dB steps
 - Single-pin antenna: no RF matching or RX/TX switching required
 - RSSI (1dB resolution)
 - Antenna array and optional off-chip RF PA/LNA control interface
- AES-128 encryption hardware
- Link layer hardware
 - Automatic packet assembly
 - Automatic packet detection and validation
 - Auto Re-transmit
 - Auto ACK
 - Hardware Address Matching
 - Random number generator
- Operating temperature: -40 °C~85°C
- RoHS Package: TSSOP16
- Applications: wearables, beacons, home and building, health and medical, industrial and manufacturing, retail and payment, data transmission, PC/mobile/TV peripherals, internet of things (IoT)

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1 Introduction

ST17H66 is a System on Chip (SoC) for Bluetooth® low energy applications. It has high-performance low-power 32-bit processor with 64K retention SRAM, 512/256KB flash, 96KB ROM, 256bit efuse, and an ultra-low power, high performance, multi-mode radio. Also, ST17H66 can support BLE with security, application and over-the-air download update. Serial peripheral IO and integrated application IP enables customer product to be built with minimum bill-of-material (BOM) cost.

2 Product Overview

2.1 Block Diagram

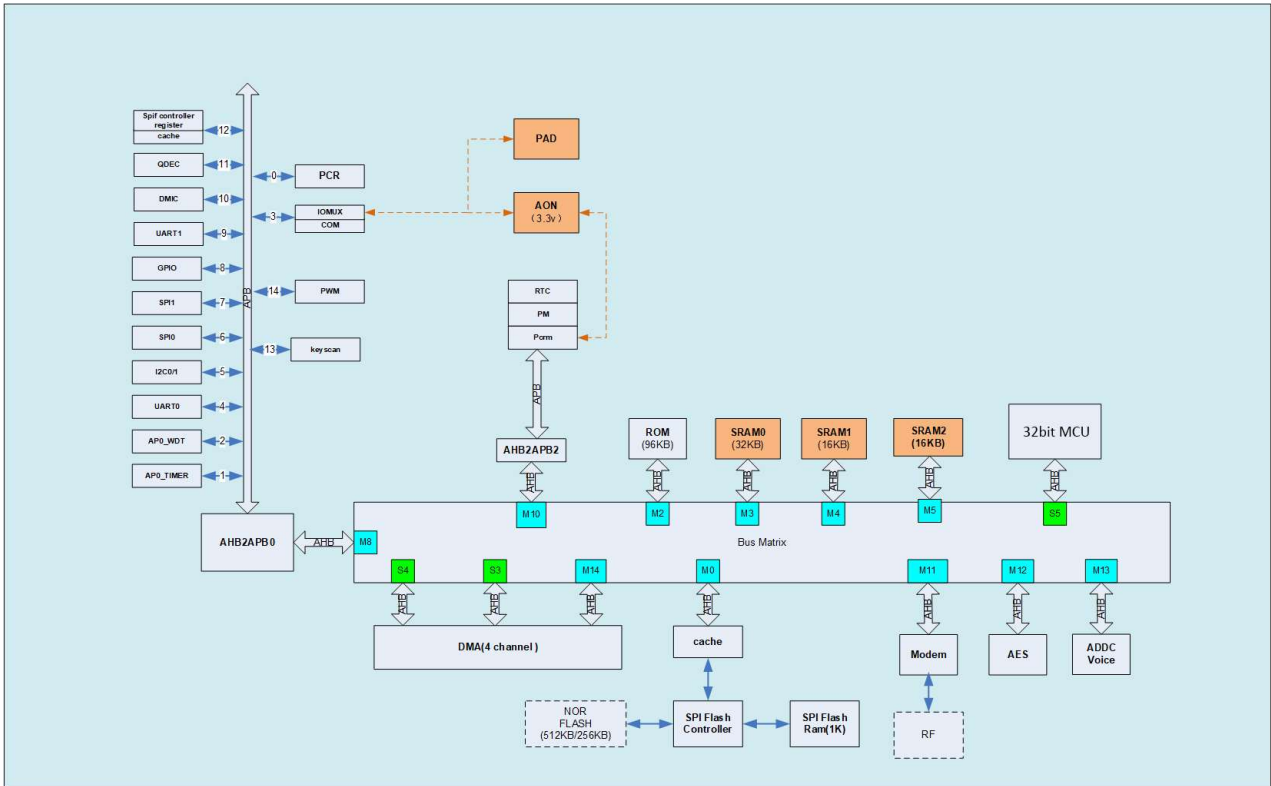


Figure 1: ST17H66 block diagram

2.2 Pin Assignments and Functions

This section describes the pin assignment and the pin functions for the package type of TSSOP16.

2.2.1 ST17H66 (TSSOP16)

2.2.1.1 Pin Assignment

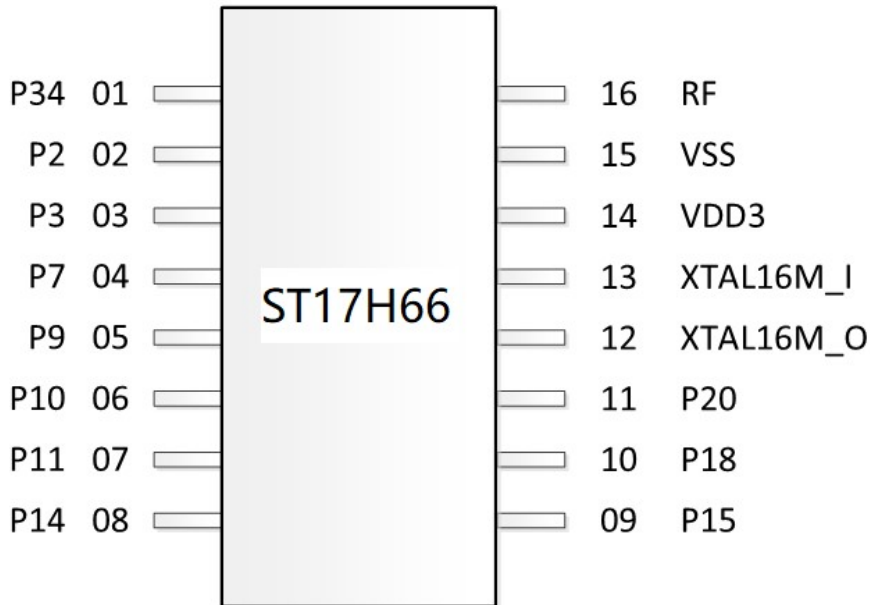


Figure 2: Pin assignment – ST17H66 TSSOP16 package

2.2.1.2 Pin Functions

Pin	Pin name	Description
1	P34	GPIO 34
2	P2	GPIO 2
3	P3	GPIO 3
4	P7	GPIO 7
5	P9	GPIO 9
6	P10	GPIO 10
7	P11 / AIO_0	GPIO 11 / ADC input 0
8	P14 / AIO_3	GPIO 14 / ADC input 3
9	P15 / AIO_4	GPIO 15 / ADC input 4 / micbias output
10	P18 / AIO_7	GPIO 18 / ADC input 7 / PGA negative input
11	P20 / AIO_9	GPIO 20 / ADC input 9 / PGA positive input
12	XTAL16M_O	16MHz crystal output
13	XTAL16M_I	16MHz crystal input
14	VDD3	3.3V power supply
15	VSS	GND
16	RF	RF antenna

*Note: All gpio support 1M/150kΩ pull up, 150kΩ pull down.

Table 1: Pin functions of ST17H66 TSSOP16 package

3 System Block

The system block diagram of ST17H66 is shown in **Figure 1**.

3.1 CPU

The ST17H66 has an high-performance low-power 32-bit processor. The CPU, memories, and all peripherals are connected by AMBA bus matrix.

The CPU will play controller role in BLE modem and run all user applications.

3.2 Memory

ST17H66 has total 96KB ROM, 64KB SRAM, 512/256KB FLASH and 256bit efuse. The physical address space of these memories is shown in **Figure 3**.

Prime Memory Space

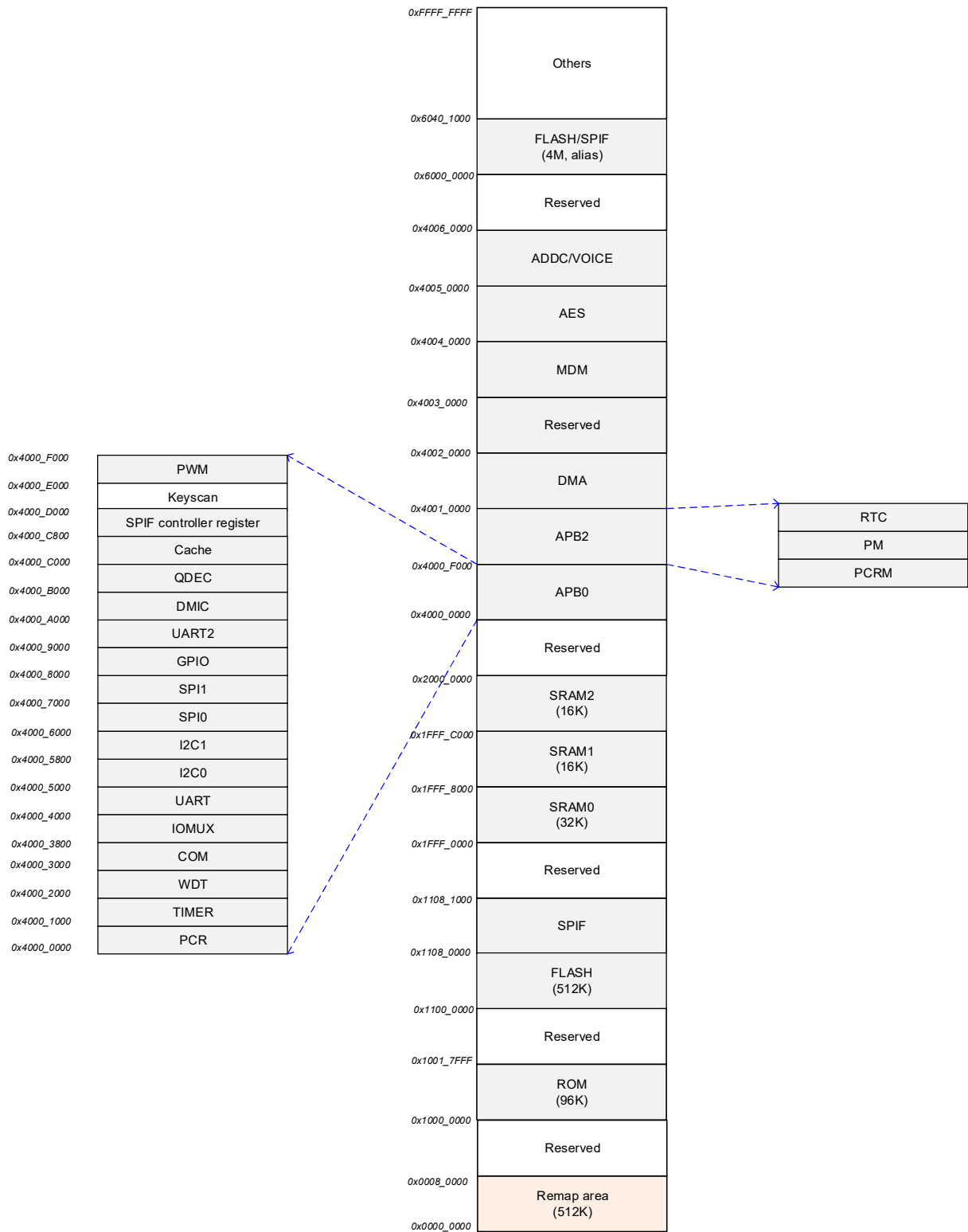


Figure 3: ST17H66 memory space

3.2.1 ROM

ST17H66 has 1 ROM.

	SIZE	CONTENT
ROM	96KB	Boot ROM. Protocol stack. Common peripheral drivers. ATE AT command.

Table 2: List of ROM

3.2.2 SRAM

ST17H66 has 5 SRAM blocks. All 5 SRAM blocks have retention capability, which can be configured individually. Normal operating voltage is 1.2V, and the voltage is adjustable at retention. All SRAM blocks can be used to store program or data.

	SIZE	CONTENT
SRAM0	32KB	
SRAM1	16KB	
SRAM2	16KB	
SRAM_BB	4KB	
SRAM_cache	8KB	

Table 3: List of SRAMs

3.2.3 FLASH

The size of FLASH can be 512KB or 256KB. Supports single-wire and 2-wire reading, 2 wire reading mode by default.

3.2.4 eFuse

ST17H66 integrates 256bits internal nonvolatile one-time programmable EFUSE storage. With a serial interface, 1-bit can be programmed at one clock in program mode and 1-bit can be read at one time in read mode.

3.2.5 Memory Address Mapping

Name	Size (KB)	Master	Physical Address
ROM	96	MCU	1000_0000~1001_7FFF
RAM0	32	MCU	1FFF_0000~1FFF_7FFF
RAM1	16	MCU	1FFF_8000~1FFF_CFFF
RAM2	16	MCU	1FFF_D000~1FFF_FFFF
FLASH	512	MCU	1100_0000~1107_FFFF 6000_0000~603F_FFFF

Table 4: Memory address mapping

3.3 Boot and Execution Modes

Only in CP Chip form, the chip enters CP boot mode after power on. ROM1 is then aliased to the 0x0 address and the chip program starts from ROM1.

Boot

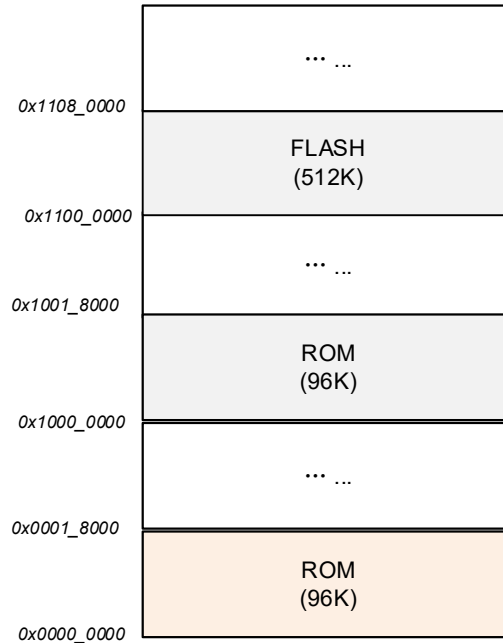


Figure 4: ST17H66 boot mode

3.3.1 Boot Loader

The boot loader in the ROM has the basic structure as shown below. The content in the FLASH should be specifically defined to allow boot loader to identify whether the FLASH content is valid, as shown in the example below. If the FLASH is valid, the ROM boot loader will put the chip in the normal mode and start normal program execution. If the FLASH is not valid, the boot loader will enter FLASH programming mode.

Address	Variable	Content
0	PRODUCT_MODE	Identify the chip mode
4	CODE_BASE	The base address of the code
8	CODE_LEN	The length of the code
C	BOOT_MODE	Identify mirror or FLASH mode

Table 5: Flash content example

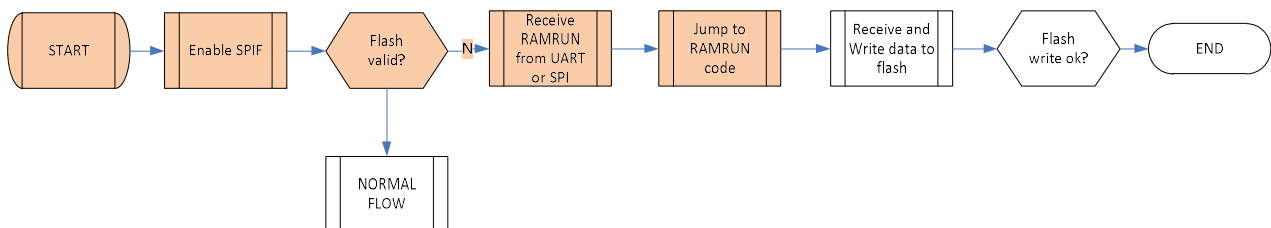


Figure 5: Bootloader flow

3.4 Power, Clock and Reset (PCR)

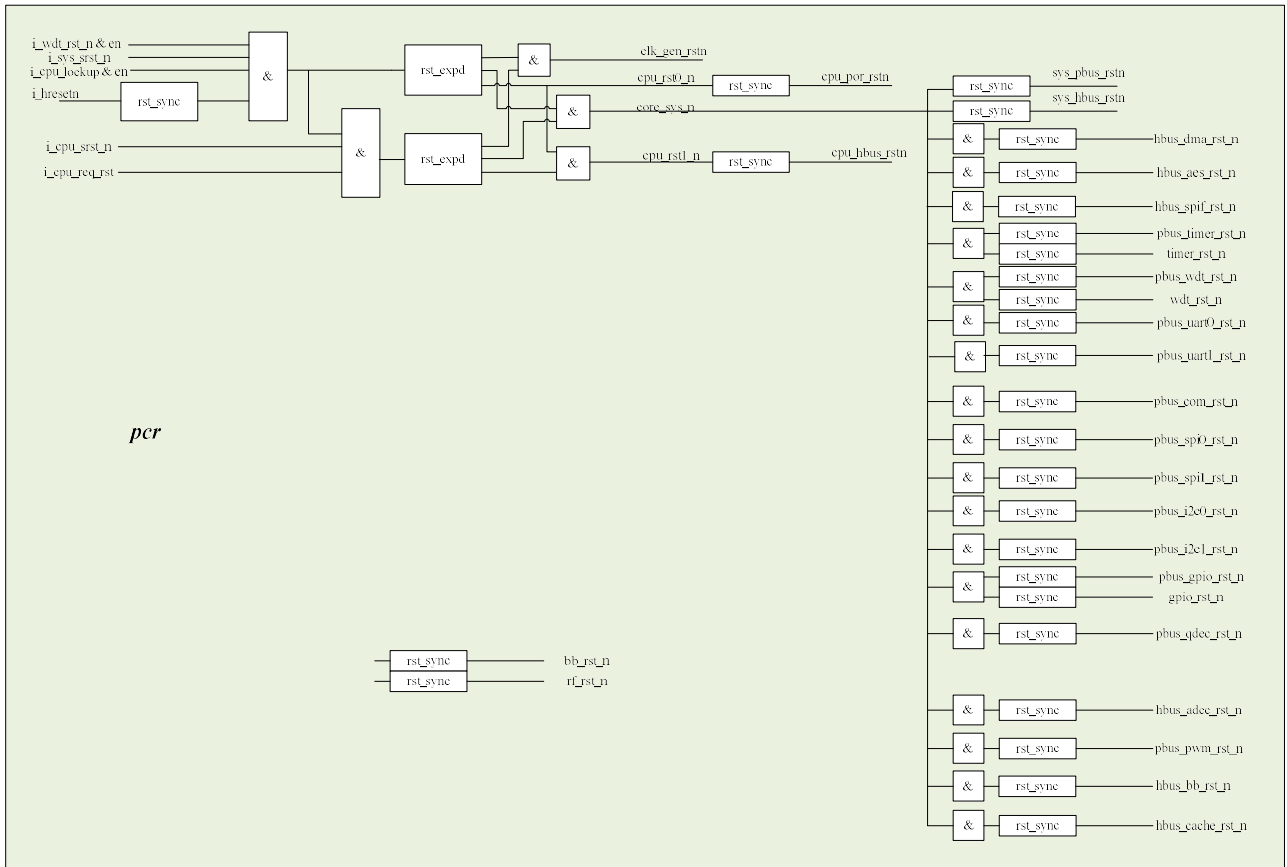


Figure 6: ST17H66 power, clock and reset

3.5 Power Management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals saving separate power state control in addition to the System Sleep mode and OFF modes. When in System Normal mode, all functional blocks will independently be turned on depending on needed application functionality.

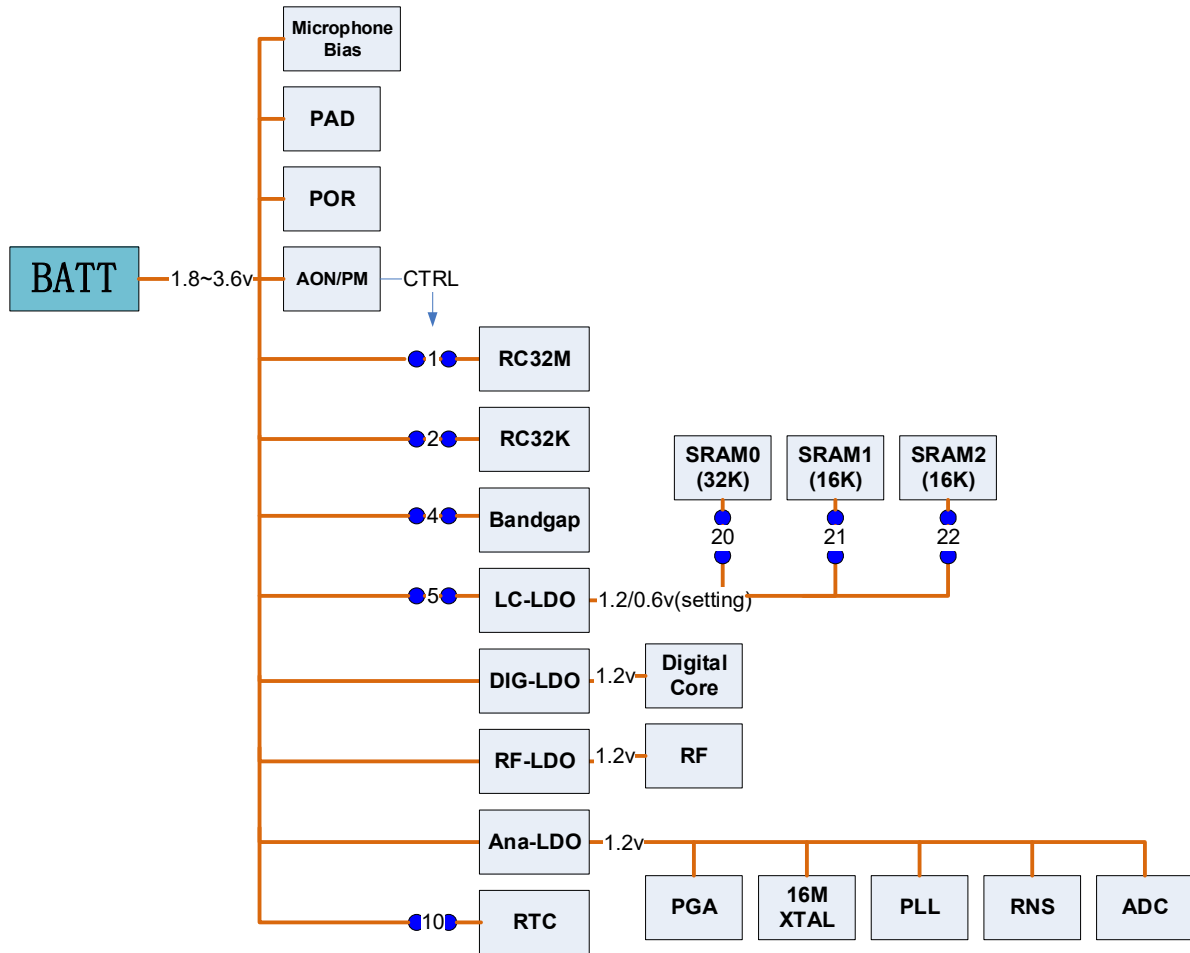


Figure 7: Power system

The following diagram is Normal, Sleep and Off mode. Switches are optional depending on user's request.

Switch	Normal	Sleep	Off
1RC32M	On	Off	Off
2RC32K	On	Optional	Off
4bandgap	On	Off	Off
5LC-LDO	On	On	Off
10RTC	On	Optional	Off
20SRAM-32K	1.2v	0.6v	0
21SRAM-16K	1.2v	0.6v	0
22SRAM-16K	1.2v	0.6v	0

Table 6: Flash Switches of different power modes

3.6 Low Power Features

3.6.1 Operation and Sleep States

3.6.1.1 Normal State

3.6.1.2 Clock Gate State

The CPU executes WFI/WFE to enter clock gate state. After wake-up from clock-gate state, the CPU continues to execute the program from where it stopped. The wake-up sources includes interrupts and events. The wake-up sources are configured by the software according to applications.

3.6.1.3 System Sleep State

The wake-up sources include:

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 System Off State

The wake-up sources include:

- IOs
- RESET
- UVLO reset

3.6.2 State Transition

3.6.2.1 Entering Clock Gate State and Wake-up

CPU executes WFI/WFE.

3.6.2.2 Entering Sleep/off States and Wake-up

The PM registers identify whether the CPU is in mirror mode or FLASH mode before sleep or off, and record the remap and vectors. The CPU configures the corresponding PM registers to put the chip into sleep mode. After wake-up, the chip enters boot mode to execute boot code in the ROM. The ROM code checks the mode before sleep/off and the remap information, perform corresponding configurations, and starts to execute the program.

3.7 Interrupts

Interrupt Name	MCU Interrupt Number
	0
MCU(coretimeirq)	1
	2
	3
bb_irq	4
kscan_irq	5
rtc_irq	6
cpcom_ap_ipc_irq	7
apcom_ap_ipc_irq	8
	9
wdt_irq	10
uart0_irq	11
i2c0_irq	12
i2c1_irq	13
spi0_irq	14
spi1_irq	15
gpio_irq	16
uart1_irq	17
spif_irq	18
dmac_intr	19
timer_irq[1]	20
timer_irq[2]	21
timer_irq[3]	22
timer_irq[4]	23
timer_irq[5]	24
timer_irq[6]	25
	26
	27
aes_irq	28
adcc_irq	29
qdec_irq	30
	31

Table 7: Interrupts

3.8 Clock Management

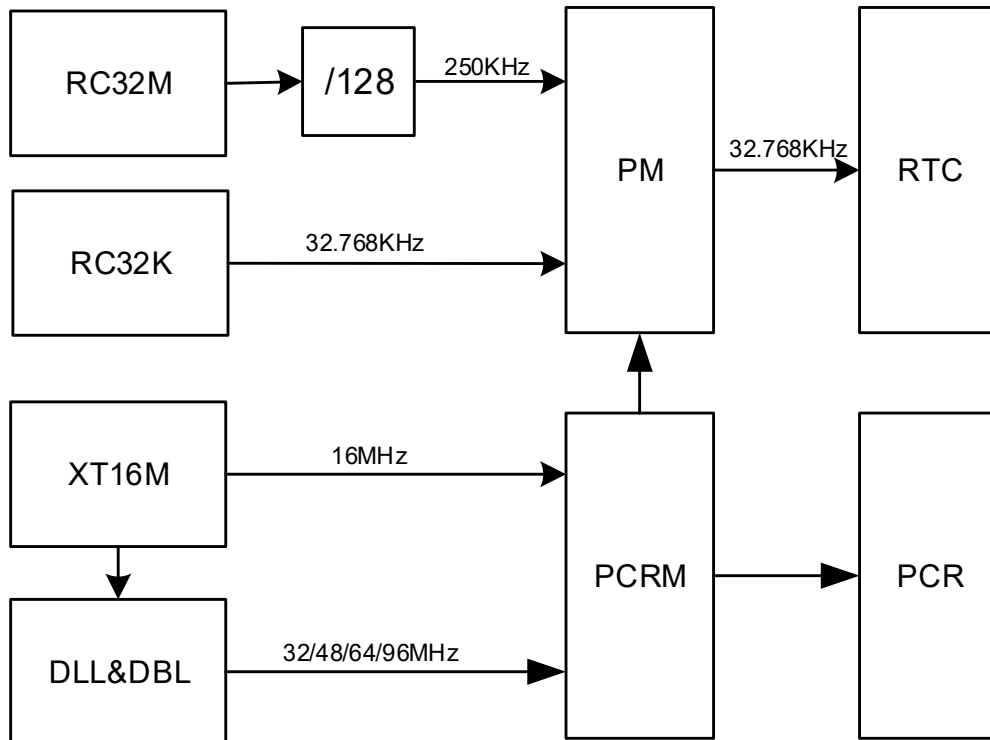


Figure 8: Clock management

There is only one crystal clock sources: 16MHz crystal oscillator (XT16M). There are also two on chip RC oscillators: 32MHz RC oscillator (RC32M) and 32kHz RC oscillator (RC32k), both of which can be calibrated with respect to 16MHz crystal oscillator. At initial power up or wake up before XT16M oscillator starts up, RC32M is used as the main clock. An on-chip DLL generates higher frequency clocks such as 32/48/64/96MHz.

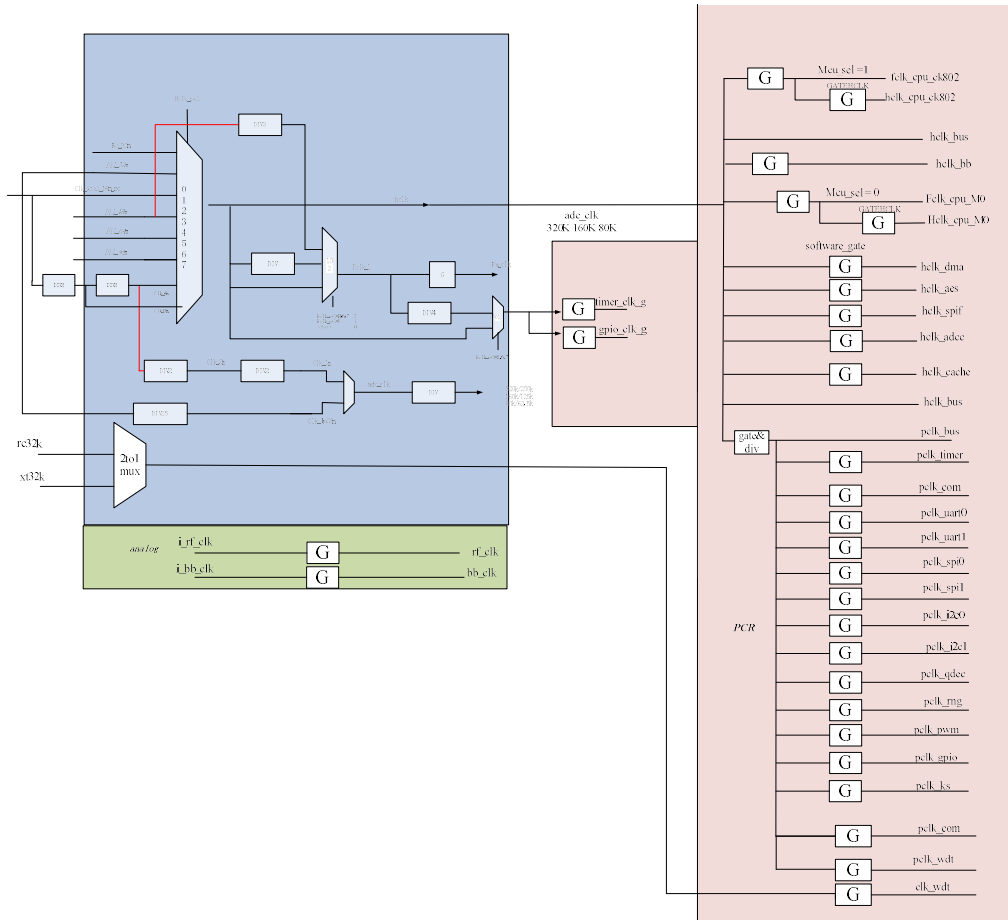


Figure 9: Clock structure diagram

3.9 IOMUX

The IOMUX provides a flexible I/O configuration, as the ports of most of the peripherals can be configured and mapped to any of the physical I/O pads (I/O at die boundary). These peripheral modules include I2C 0-1, UART0-1, PWM 0-5, SPI 0-1, Quadrature Decoder etc. However for other specific purpose peripherals, their IOs mappings are fixed when they are enabled. These specific purpose peripherals include JTAG, analog_ios, GPIOs and key scan.

Figure 10 below shows the IOMUX functional diagram.

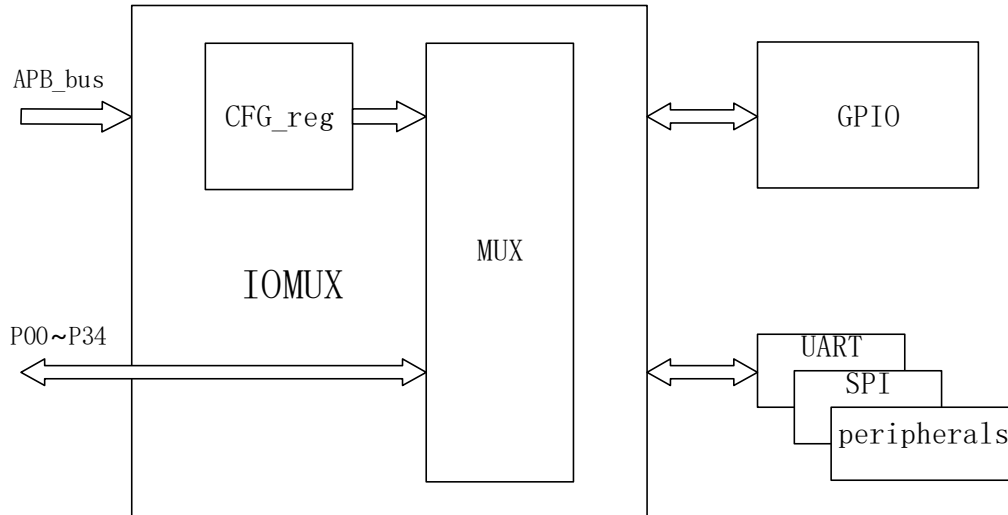


Figure 10: IOMUX structure diagram

There are 11 configurable pads. The table below shows the mapping of the peripheral IOs that can be mapped through IOMUX. These include I2C 0-1, I2S, UART, PWM 0-5, SPI 0-1, Quadrature Decoder, 1.28MHz clock and dmic_out.

On the other hand, there are also special purpose peripherals, whose IOs are fixed to certain physical pads, when these peripheral functions are enabled. These special purpose peripherals include: JTAG, analog I/Os (ADC inputs), GPIO, and key scan. When they are enabled, their IOs are mapped to physical pads according to the following table.

#	SOP16			Name
0	GPIO_P34	GPIO		mk_in[8]
1	GPIO_P02	GPIO		mk_in[1]
2	GPIO_P03	GPIO		mk_out[1]
3	GPIO_P07	GPIO		mk_in[10]
4	GPIO_P09	GPIO		mk_out[4]
5	GPIO_P10	GPIO		mk_in[4]
6	GPIO_P11	GPIO	analog_io[0]	mk_out[11]
7	GPIO_P14	GPIO	analog_io[3]	mk_out[2]
8	GPIO_P15	GPIO	analog_io[4]	mk_in[2]
9	GPIO_P18	GPIO	analog_io[7]	mk_in[5]
10	GPIO_P20	GPIO	analog_io[9]	mk_out[5]

Table 8: Peripheral IO mapped through IOMUX (special purpose)

3.10 GPIO

The General Purpose I/Os are a type of peripheral that can be mapped to physical I/O pads and programmed by software. The flexible GPIO are organized as PORT A. PortA has bi-direction 18 bit lines, e.g., GPIO_PORT A[22:0]. With default setting, physical pads: P00-P34 are connected to PortA. When all GPIOs are enabled, as described in the IOMUX table in IOMUX section.

All PortA pins can be configured as bi-directional serial interface, by selecting as input or output direction, and their corresponding data can be either read from or written to registers. All PortA and pins support wake-up and debounce function, but only 18 PortA pins support interrupt.

Each GPIO pins can be pulled up to VDD3 or pulled down to ground by adding pull up or pull down resistors to have default functions/states.

For more detailed info, please refer to “ST17H6x GPIO Application Notes”, in software SDK document folder.

#	SOP16	Default MODE	Default IN_OUT	IRQ	Wakeup	ANA_IO
0	GPIO_P34	GPIO	IN	√	√	
1	GPIO_P02	GPIO	IN	√	√	
2	GPIO_P03	GPIO	IN	√	√	
3	GPIO_P07	GPIO	IN	√	√	
4	GPIO_P09	GPIO	IN	√	√	
5	GPIO_P10	GPIO	IN	√	√	
6	GPIO_P11	GPIO	IN	√	√	ADC_CH1N_P11
7	GPIO_P14	GPIO	IN	√	√	ADC_CH2P_P14
8	GPIO_P15	GPIO	IN	√	√	ADC_CH3N_P15
9	GPIO_P18	GPIO	IN	√	√	
10	GPIO_P20	GPIO	IN	√	√	ADC_CH3P_P20

Table 9: ST17H66 GPIO Application Notes

3.10.1 DC Characteristics

TA=25°C, VDD=3 V

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
Logic-0 output voltage, 10-mA pins	Output load 10 mA			0.5	V
Logic-1 output voltage, 10-mA pins	Output load 10 mA	2.5			V

Table 10: DC Characteristics

4 Peripheral Blocks

4.1 2.4GHz Radio

The 2.4 GHz RF transceiver is designed to operate in the worldwide ISM frequency band at 2.4 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with *Bluetooth*[®] low energy (BLE) protocol implementations.

- General modulation format
 - FSK (configurable modulation index) with configurable Gaussian Filter Shaping
 - OQPSK with half-sine shaping
 - On-air data rates
 - 125kbps/250kbps/500kbps/1Mbps/2Mbps
- Transmitter with programmable output power of -20dBm to +10dBm, in 3dB steps
- RSSI function (1 dB resolution, ± 2 dB accuracy)
- Receiver sensitivity
 - -103dBm@125Kbps GFSK
 - -98dBm@500Kbps GFSK
 - -97dBm@1Mbps BLE
 - -94dBm@2Mbps BLE
- Embedded RF balun
- Integrated frac-N synthesizer with phase modulation

4.2 Timer/Counters (TIMER)

The implementation can include a 32-bit SysTick system timer, that extends the functionality of both the processor and the NVIC. When present, the NVIC part of the extension provides:

- A 32-bit system timer (SysTick)
- Additional configurable priority SysTick interrupt.

General purpose timers are included in the design. With the input clock running at 4Mhz.

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

4.4 AES-ECB Encryption (ECB)

The ECB encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

4.5 Watchdog Timer (WDT)

A count down watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.6 SPI (SPI0, SPI1 Two Independent Instances)

The SPI interface supports 3 serial synchronous protocols which are SPI, SSP and Microwire serial protocols. SPI wrapper contains one SPI master and one SPI slave. They are logically exclusive. Only one block is alive at a time. The operation mode for master mode and slave mode is controlled by PERI_MASTER_SELECT Register in COM block.

bit	Reset value	Definition
1	0	SPI1 is master mode when set
0	0	SPI0 is master mode when set

Table 11: PERI_MASTER_SELECT Register bit definition
(base address = 0x4000_302C)

4.7 I2C (I2c0, I2c1 Two Independent Instances)

This I2C block support 100Khz, and 400Khz modes. It also supports 7-bit address and 10-bit address. It has built-in configurable spike suppression function for both lines.

4.8 UART (UART0, UART1 Two Independent Instances)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin out and enables efficient use of board space and signal routing.

4.9 DMIC/AMIC Data Path

The voice in interface supports one analog MIC (SAR-ADC) and two digital MIC (L+R), different output sample rate (64KHz, 32KHz, 16KHz and 8KHz), and different voice compress algorithm. For the Digital MIC, PDM signal is sampled at 1.28MHz(4x320KHz). L channel is sampled at raising edge, R channel is sampled at falling edge. For PCM-LOG and CVDS, output data rate is 64Kbps (8KHz x 8bit).

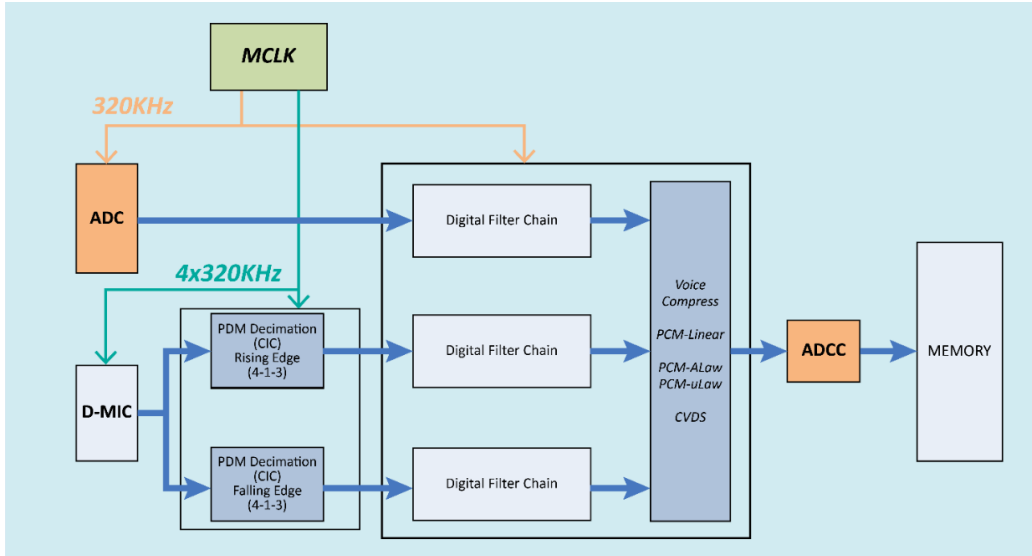


Figure 11: Block Diagram of Voice In Interface

4.9.1 Filter Chain Design

For D-MIC input, PDM Decimation (CIC) will convert the 1-bit PDM signal to 12 bit PCM signal. And the sample rate will be converted from 1.28MHz to 320KHz. The output data of the PDM Decimation will be connected to the Digital Filter chain.

For the A-MIC input, SAR-ADC will convert the signal to 12bit 320KHz digital samples. The Digital Filter chain will process the data same as the D-MIC path.

The Output sample rate of the Digital filter chain is programmable. 64KHz, 32KHz, 16KHz, 8KHz. The maximum value of the sample's bit-width is 16bit.



Figure 12: Digital Filter Chain

4.9.2 Auto Mute Process

Signal Level Estimate will check the input signal level with configurable window size. Mute threshold can be updated according to the signal level estimation or being configured by the register. There are two thresholds, one for MUTE_ON, another for MUTE_OFF. Gain step of MUTE_ON and MUTE_OFF can be configured individually.

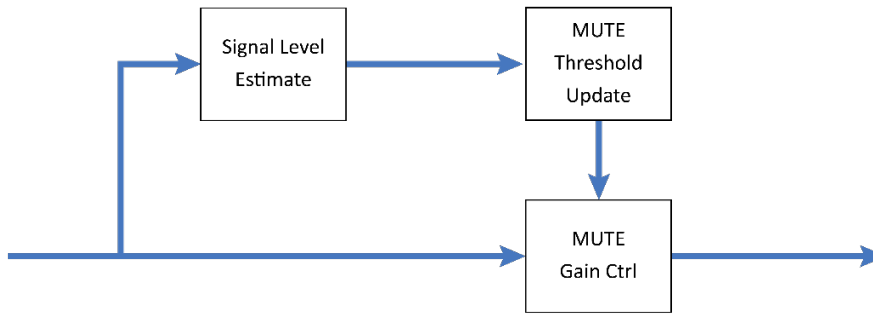


Figure 13: Auto Mute Process

4.9.3 Digital Gain Control

Digital gain is implemented by one Look up table. The gain error has been controlled within 0.05dB.

4.9.4 Voice Compression

PCM-LOG support u-Law and a-Law. According to the ITU-G711 standard. The input data is 13~14bit @ 8KHz. The output data is 8bit @ 8KHz, 64Kbps. Also, it support 64Kbps CVSD according to the BT standard. Its Input is 16bit @64KHz, and its output is 1bit @ 64KHz. PCM-Linear is for the raw data without compression.

4.10 Pulse Width Modulation (PWM)

ST17H6x supports 6 channels of Pulse Width Modulation (PWM) outputs. PWM outputs generate waveforms with variable duty cycle or pulse width programmed by registers. And each of the 6 PWM outputs can be individually programmed. Their duty cycles are controlled by programming individual counters associated with each channel.

The master clock is 16MHz. For each PWM outputs, first there is a prescaler (pre-divider) with division ratio of 2 to 128 (only 2^N division ratios are supported), followed by another 16bit counter with programmable max count, denoted as top_count. When the 16bit counter counts from 0 to top_count, it resets back to 0. So the frequency of the PWM is given by:

$$\text{Freq_PWM} = 16\text{MHz} / (N_{\text{prescaler}} * N_{\text{top_count}});$$

A threshold counter number can be programmed, when the 16bit counter reaches the threshold, PWM output toggles. So the duty cycle is:

$$\text{Duty_cycle_PWM} = N_{\text{threshold}}/N_{\text{top_count}};$$

The polarity of the PWM can also be programmed, which indicates output 1 or 0 when counter is below/above the threshold. A PWM waveform vs counter values are illustrated in the following **Figure 15**, where the polarity is positive. Also in this case the counter ramps up and then resets, we call it “up mode”.

There is also a “up and down mode”, where the counter ramps up to count_top and then ramps down, instead of reset.

As discussed above, the key register bits for one PWM channel are: 16bit top_count, 16bit threshold count, 3bit prescaler count, PWM polarity, PWM mode (up or up/down), PWM enable, and PWM load enable (load new settings). All 6 PWM channels can be individually programmed by registers with addresses from 0x4000_E004 to 0x4000_E044. In addition, one should enable registers

0x4000_E000<0><4> to allow all PWM channels can be programmed. For details please refer to documents of ST17H6x register tables.

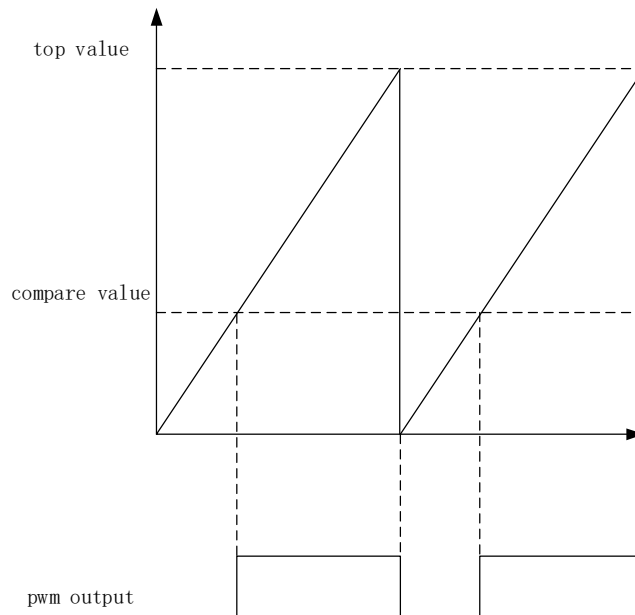


Figure 14: PWM operation

4.11 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals with input debounce filters. It is suitable for mechanical and optical sensors. The sample period and accumulation are configurable to match application requirements. The quadrature decoder has three-axis capability and index channel support. It can be programmed as 4x/2x/1x count mode.

4.12 Key Scan (KSCAN)

Keyscan supports key matrix with upto 16 rows by 18 columns. Each individual rows or columns can be enabled or disabled through register settings. GPIO pins can be configured to be used for key scan. A few key scan Parameters can be set through registers, including polarity (low or high indicating key pressed); support multi-key-press or only single-key-press; de-bounce time (the time duration a key press is deemed valid) from 0 to 128mS with 255us step.

A valid key press can trigger an interrupt when keyscan interrupt is enabled. After a keyscan interrupt is serviced, writing 1 to the interrupt state register bit can clear the state bit.

The keyscan has a manual mode and an auto mode. For manual mode, when a keyscan interrupt is received, it is up to the MCU/software to scan the keyscan output pins and check the input pins, to determine which keys have been pressed. Manual mode is relatively slow and need CPU to process. On the contrary, in automodekeyscan will automatically scan the output/input pins, and store the row/column info corresponding to the key pressed into read only registers, then trigger an interrupt for software to retrieve key press information.

4.13 Analog to Digital Converter (ADC) with Programmable Gain Amplifier (PGA)

The 12bit SAR ADC has total 10 inputs. Among them, there are two for PGA inputs, and two differential inputs for the on-chip temperature sensor. The other six inputs can be programmed to 3 pair differential inputs or six single-ended inputs. There is a manual mode with which the ADC can be configured to convert a specific input in single-ended or differential and with a specific ADC clock rate. There is also an auto sweep mode, namely all enabled input channels can be swept automatically in order by the ADC and the converted data will be stored at corresponding memory locations.

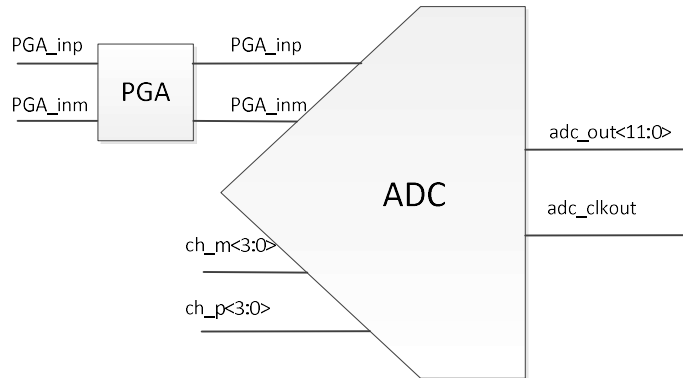


Figure 15: ADC

4.13.1 PGA Path

The PGA provides 42dB gain range from 0dB to 42dB in 3dB steps.

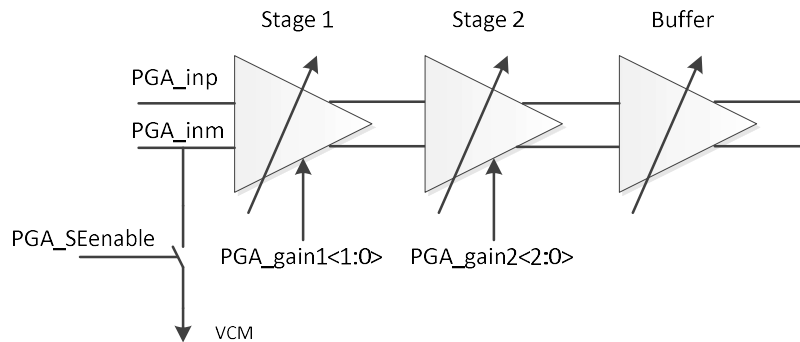


Figure 16: PGA path

pga_gain1<1>	pga_gain1<0>	Stage1 gain (dB)	pga_gain2<2>	pga_gain2<1>	pga_gain2<0>	Stage2 gain(dB)
0	0	0	0	0	0	0
0	1	12	0	0	1	3
1	0	24	0	1	0	6
			0	1	1	9
			1	0	0	12
			1	0	1	15
			1	1	0	18

Table 12: PGA gain

Set PGA_SEenable to "1", PGA will be set to Single-ended mode by pulling the PGA into its Common-

mode voltage.

4.13.2 ADC Path

By default the ADC is configured in manual mode. In this mode, the ADC clock rate can be configured to 80k/160k/320k sample per second. Select the pair of inputs and configure it to differential or singled-ended (positive or negative). By default it is differential. After enabling, the ADC will take samples with the configured clock rate and store the data to a channel dependent memory location. For each channel a memory size of 128Byte is allocated, when it is full an interrupt bit will be flagged. Each sample of 12bits takes 2 Byte memory space.

ADC can also be configured into auto channel sweep mode by setting the “adc_ctrl_override” bit to 0, with which the enabled channels will be sampled in the configured order automatically. The ten ADC input channels can be configured by programming their corresponding registers. Their configurations include sampling time, enable/disable, differential/single-ended, and continuous sampling/single-shot, based on the following register table. The sampled data is stored in the corresponding memory locations as in manual mode.

0x4000_F06C	ADC_CTL0	Register Description
[31:16]	Temperature sensing, auto mode, differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	PGA inputs, differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x4000_F070	ADC_CTL1	Register Description
[31:16]	Inputs A, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	Input A, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x4000_F074	ADC_CTL2	Register Description
[31:16]	Input B, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

[15:0]	Input B, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x4000_F078	ADC_CTL3	Register Description
[31:16]	Input C, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	Input C, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

Table 13: ADC channel configurations

4.13.3 ADC Channel <3:0> Connectivity

PGA inputs	hardwired
aio<0>	Input A negative
aio<1>	Input A positive
aio<2>	Input B negative
aio<3>	Input B positive
aio<4>	Input C negative
aio<9>	Input C positive
aio<7>	Input D positive
aio<8>	Input D negative

Table 14: ADC channel connectivity

Aio<9, 4:0> and PGA inputs(Aio<7:8>) can be selected through an analog Mux by programming aio_pass<7:0> or aio_attn<7:0>. For example, register 0x4000_F020<8><0> set to 01, then Aio<0> is connected to ADC input A positive node.

0x4000_F020		Register Description
[13:8]	Attenuation ctrl	attn[5:0]. analogIO control for {aio<9>, aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass 10 attenuate to 1/4 11 NC
[5:0]	pass ctrl	pass[5:0]. analogIO control for {aio<9>, aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass 10 attenuate to 1/4 11 NC note: analog IO sharing gpio<11>/aio<0> gpio<12>/aio<1> gpio<13>/aio<2> gpio<14>/aio<3> gpio<15>/aio<4> gpio<16>/aio<5>/32K XTAL input gpio<17>/aio<6>/32K XTAL output gpio<18>/aio<7>/pga in+ gpio<19>/aio<8>/pga in- gpio<20>/aio<9>/mic bias

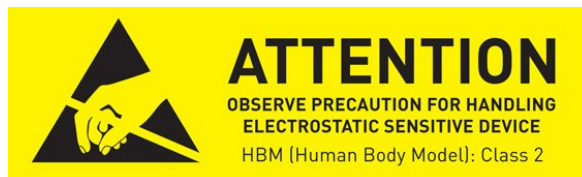
Table 15: analog Mux

5 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which ST17H66 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the ST17H66. **Table 16** specifies the absolute maximum ratings for ST17H66.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
DEC			1.32	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
	Storage temperature	-40	+85	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model Class 2		8	kV
ESD CDMQF	Charged Device Model (TSSOP16, 5x4.4 mm package)		500	V
Flash memory				
	Endurance		100 000	write/erase cycles
	Retention		10 years at 40 °C	
	Number of times an address can be written between erase cycles		2	times

Table 16: Absolute maximum ratings



6 Operating Conditions

The operating conditions are the physical Parameters that ST17H66 can operate within as defined in **Table 17**.

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
tr_VDD	Supply rise time (0 V to 1.8 V)			100	ms
TA	Operating temperature	-40	27	85	°C

Table 17: Operating conditions

7 Radio Transceiver

7.1 Radio Current Consumption

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	@3V		8.6		mA
Rx Only	@3V		8		mA

Table 18: Radio current consumption

7.2 Transmitter Specification

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			10		dBm
RF Min Output Power			-20		dBm
OBW for BLE 1Mbps	20dB occupy-bandwidth for BLE modulation 1Mbps		1100		KHz
OBW for BLE 2Mbps	20dB occupy-bandwidth for BLE modulation 2Mbps		2300		KHz
OBW for GFSK 500Kbps	20dB occupy-bandwidth for GFSK modulation 2Mbps		1100		KHz
OBW for GFSK 125Kbps	20dB occupy-bandwidth for GFSK modulation 2Mbps		1100		KHz
Error Vector Measure	Offset EVM for OQPSK modulation		0.02		
FDEV for BLE 1Mbps	Frequency deviation for GFSK modulation 1Mbps	160		250	KHz
FDEV for BLE 2Mbps	Frequency deviation for GFSK modulation 2Mbps	320		500	KHz

Table 19: Transmitter specification

7.3 Receiver Specification

7.3.1 RX BLE 1Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-97		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		7		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >= +/- 5MHz, 37 Byte BER=1E-3		55		I/C dB

Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3	22	I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3	-20	dBm
Carrier Frequency Offset Tolerance		+ 350	KHz
Sample Clock Offset Tolerance		+ 120	ppm

Table 20: RX BLE 1Mbps GFSK

7.3.2 RX BLE 2Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 2Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-94		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +/-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-5		I/C dB
Selectivity +/-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		9		I/C dB
Selectivity +/-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		30		I/C dB
Selectivity +/-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		40		I/C dB
Selectivity +/-5MHz or More	Wanted signal at -67dBm, modulated interferer at >= +/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+ 350		KHz
Sample Clock Offset Tolerance			+ 120		ppm

Table 21: RX BLE 2Mbps GFSK

7.3.3 RX 500Kbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 500Kbps BLE ideal transmitter, 37 Byte BER=1E-3		-98		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-4		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		10		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		24		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte Ber=1E-3		-19		dBm
Carrier Frequency Offset Tolerance			+350		KHz
Sample Clock Offset Tolerance			+120		ppm

Table 22: RX 500Kbps GFSK

7.3.4 RX 125Kbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 125Kbps BLE ideal transmitter, 37 Byte BER=1E-3		-103		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-1		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-11		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		28		I/C dB

Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3	-18	dBm
Carrier Frequency Offset Tolerance		+/- 350	KHz
Sample Clock Offset Tolerance		+/- 120	ppm

Table 23: RX 125Kbps GFSK

7.4 RSSI Specifications

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

Table 24: RSSI specifications

8 Glossary

Term	Description
AHB	Advanced High-performance Bus
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

Table 25: Glossary

9 Ordering information

Part#	Order Info	Internal Memory	Package	Temperature range	MOQ
ST17H66	ST17H66B2	256KB Flash, 64K SRAM	TSSOP16 /Tube	-40° ~ 85°	3000pcs

Table 26: Ordering information

10 Package dimensions

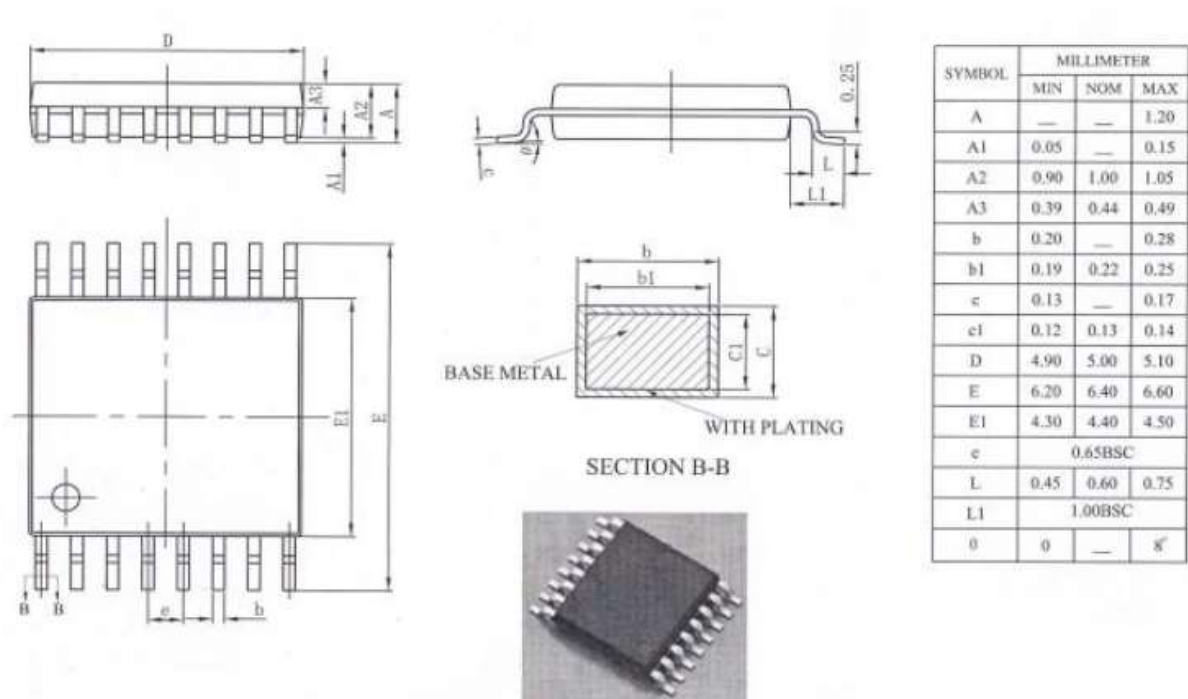


Figure 17: TSSOP16 package dimensions

Note: dimensions are in mm, angels are in degree.

11.2.2 Bypass Capacitor

1. Each VDD pin needs a bypass capacitor to release chip internal noise and block noise from power supply.
2. For power traces, bypass capacitors should be placed as close as possible to VDD pins.
3. Use one large and one small capacitor when the pin needs two capacitors. Typically the capacitance of the larger capacitor is about 100 times of that of the smaller one. The smaller capacitor usually has better quality factor than the larger one. Place the larger capacitor closer to the pin.
4. The capacitors of Loop filter need to have larger clearance to prevent EMC/EMI issue.
5. Ground via should be close to the Capacitor GND side, and away from strong signals.

11.2.3 Layer Definition

1. Normally 4 layer PCB is recommended.
2. RF trace must be on the surface layer, i.e. top layer or bottom.
3. The second layer of RF PCB must be "Ground" layer, for both signal ground and RF reference ground, DO NOT put any other trace or plane on second layer, otherwise "antenna effect" will complicate debug process.
4. Power plane generally is on the 3rd layer.
5. Bottom layer is for "signal" layer.
6. If two layer PCB is used, quality will degrade in general. More care needs to be taken. Try to maximize ground plane, avoid crossing of signal trace with other noise lines or VDD, shield critical signal line with ground plane, maximize bypass capacitor and number of ground vias.

11.2.4 Reference clock and trace

1. Oscillator signal trace is recommended to be on the 1st layer;
2. DO NOT have any trace around or across the reference clock (oscillator) trace.
3. Isolate the reference clock trace and oscillator by having more GND via around.
4. DO NOT have any other traces under the Oscillator.

11.2.5 Power line or plane

1. Whether to use power plain or power line depend on the required current, noise and layout condition. For RF chip, we generally suggest to use power line to bring power into IC pin. Line has parasitic inductance, which forms a low pass filter to reduce the noise traveling around PCB.
2. Add more conductive via on the current source, it will increase max current limit and reduce inductance of via.
3. Add some capacitor alone the power trace when power line travels a long distance.
4. DO NOT place power line or any plane under RF trace or oscillator and its clock trace, the strong clock or RF signal would travel with power line.

11.2.6 Ground Via

1. Ground Via must be as close to the ground pad of bypass capacitor as possible, too much distance between via and ground pad will reduce the effect of bypass capacitor.
2. Having as many ground via as possible.
3. Place ground via around RF trace, the RF trace should be shielded with via trail.